## AMENDMENT TO THE TITLE

Please delete the title in its entirety and please substitute:

--DRAM WITH SUPER SELF-REFRESH AND ERROR CORRECTION FOR EXTENDED PERIOD BETWEEN REFRESH OPERATIONS--.

## AMENDMENTS TO THE SPECIFICATION

**Please replace paragraph [0010] with the following rewritten paragraph:**

**[0010]** (1) A semiconductor integrated circuit device having a dynamic RAM, the dynamic RAM comprising a memory array, a RAM control section, an ECC-codec circuit, and an ECC controller, the RAM control section comprising a command decoding section responsive to an ~~xtemal~~ external command from the outside of the dynamic RAM for decoding the external command and a super self-refresh control circuit, wherein:

**Please replace paragraph [0012] with the following rewritten paragraph:**

**[0012]** the ECC controller ~~comprising~~ comprises a command generating section and an address generating section;

**Please replace paragraph [0013] with the following rewritten paragraph:**

**[0013]** the command decoding section ~~delivering~~ delivers a start instruction signal representative of encoding to the ECC controller when an entry command is decoded as the external command;

**Please replace paragraph [0014] with the following rewritten paragraph:**

**[0014]** the command generating section of the ECC controller ~~delivering~~ delivers, upon reception of the start instruction signal, a first operation mode signal representative of the encoding and simultaneously ~~making~~ makes the address generating section of the ECC controller sequentially generate addresses corresponding to operation timings of the first operation mode signal and ~~supply~~ supplies the addresses to the memory array;

**Please replace paragraph [0015] with the following rewritten paragraph:**

**[0015]** the ECC-codec circuit ~~carrying~~ carries out, upon reception of the first operation mode signal, an encoding operation of producing a check bit for error detection/correction with reference to information data stored in the memory array and ~~writing~~ writes the check bit into a predetermined region of the memory array;

**Please replace paragraph [0016] with the following rewritten paragraph:**

**[0016]** the command generating section of the ECC controller ~~delivering~~ delivers, upon completion of the encoding operation by the ECC-codec circuit, a first end signal as the internal command to the command decoding section;

**Please replace paragraph [0017] with the following rewritten paragraph:**

**[0017]** the super self-refresh control circuit of the RAM control section ~~starting~~ starts, when the command decoding section receives and decodes the first end signal as the internal command, a super self-refresh operation which has a refresh cycle lengthened within an allowable range of error occurrence by an error correcting operation using the check bit.

**Please replace paragraph [0019] with the following rewritten paragraph:**

**[0019]** the entry command is supplied by a user to [[th]] the dynamic RAM.

**Please replace paragraph [0021] with the following rewritten paragraph:**

**[0021]** the command decoding section ~~delivering~~ delivers, when an exit command as the external command is decoded, a stop instruction signal representative of decoding to the ECC controller;

**Please replace paragraph [0023] with the following rewritten paragraph:**

**[0023]** the command generating section of the ECC controller ~~delivering~~ delivers, upon reception of the stop instruction signal, a second operation mode signal representative of the decoding and simultaneously ~~making~~ makes the address generating section of the ECC controller

sequentially generate addresses corresponding to operation timings of the second operation mode signal and ~~supply~~ supplies the addresses to the memory array;

**Please replace paragraph [0024] with the following rewritten paragraph:**

**[0024]** the ECC-codec circuit ~~carrying~~ carries out, upon reception of the second operation mode signal, a decoding operation of reading the check bit for error detection/correction from the predetermined region of the memory array and ~~correcting~~ corrects, with reference to the check bit and the information data stored in the memory array, an error in the information data to rewrite the information data;

**Please replace paragraph [0025] with the following rewritten paragraph:**

**[0025]** the command generating section of the ECC controller ~~delivering~~ delivers, upon completion of the encoding operation by the ECC-codec circuit, a second end signal as the internal command to the command decoding section.

**Please replace paragraph [0028] with the following rewritten paragraph:**

**[0028]** (5) A semiconductor integrated circuit device ~~having~~ has a dynamic RAM, the dynamic RAM comprising a memory array, a RAM control section, an error correction circuit, and a BIST (built-in self-test) controller, the RAM control section comprising a command decoding section responsive to an external command from the outside of the dynamic RAM for decoding the external command, wherein:

**Please replace paragraph [0030] with the following rewritten paragraph:**

**[0030]** the BIST controller ~~comprising~~ comprises a command generating section and an address generating section;

**Please replace paragraph [0031] with the following rewritten paragraph:**

**[0031]** the command decoding section ~~delivering~~ delivers a start instruction signal representative of checking to the error correction circuit when a BIST entry command is decoded as the external command;

**Please replace paragraph [0032] with the following rewritten paragraph:**

**[0032]** the command generating section of the BIST controller ~~delivering~~ delivers, upon reception of the start instruction signal, an operation mode signal representative of the checking and simultaneously ~~making~~ makes the address generating section of the BIST controller sequentially generate addresses corresponding to operation timings of the operation mode signal and ~~supply~~ supplies the addresses to the memory array;

**Please replace paragraph [0033] with the following rewritten paragraph:**

**[0033]** the error correction circuit ~~producing~~ produces, upon reception of the operation mode signal, write data corresponding to the addresses sequentially generated, ~~writing~~ writes the write data into a predetermined region or an entire region of the memory array, ~~producing~~ produces expectation data corresponding to the addresses sequentially generated, ~~comparing~~ compares the expectation data with information data read from the memory array, ~~detecting~~ detects an error in the information data, and, upon completion of error detection, ~~delivering~~ delivers an end signal as the internal command to the command decoding section;

**Please replace paragraph [0035] with the following rewritten paragraph:**

**[0035]** (6) A semiconductor integrated circuit device as ~~describ d~~ described in (5), wherein:

**Please replace paragraph [0046] with the following rewritten paragraph:**

**[0046]** Fig. 9 is a view for describing a correcting operation (Correct) (1) (syndrome calculation) in an example 2 of the super self-refresh ~~int mal~~ internal operation carried out in the ECC-CODEC circuit illustrated in Fig. 6;

**Please replace paragraph [0075] with the following rewritten paragraph:**

**[0075]** Referring to Fig. 1, a semiconductor integrated circuit device according to one embodiment of this invention comprises a 64-Mb SDRAM 10 having a super self-refresh mode. The SDRAM 10 having a super self-refresh mode is a semiconductor dynamic memory for carrying out data input/output operations in synchronization with an external input clock CLK. The SDRAM 10 comprises first through fourth memory arrays (first through fourth banks #0 through #3). Among the first through the fourth banks #0 to #3, the second and the third banks #1 and #2 are not shown in the figure for convenience of illustration but are similar in structure to the first and the fourth banks #0 and #3. The semiconductor integrated circuit device has, as interfaces, clock terminals and control signal terminals including CLK (clock), CKE (clock enable), CS (chip select), WE (write enable), CAS (column address [[stobe]] strobe), and RAS (row address [[stobe]] strobe), address signal terminals including A0-A11 (memory array address) and BA0-BA1 (bank address), and data input/output signal terminals including DQM (data mask signal) and DQ0-DQ7 (data input/output signal).

**Please replace paragraph [0078] with the following rewritten paragraph:**

**[0078]** The control logic 209 comprises an input buffer circuit (COMMAND DECODE) 8 responsive to an external command as a combination of a CS (chip select) signal, a WE (write enable) signal, a CAS (column address [[nable]] enable) signal, and a RAS (row address enable) signal for decoding the external command. The input buffer circuit (COMMAND DECODE) 8 is also adapted to receive an end signal (READY) and an internal operation command 2 as an internal command and to decode the internal command.

**Please replace paragraph [0081] with the following rewritten paragraph:**

**[0081]** In the above-mentioned semiconductor integrated circuit device of Fig. [[25]] 1, the input buffer circuit (COMMAND DECODE) 8 of the control logic (CONTROL LOGIC) 209 of the SDRAM 10 decodes the external command as a combination of the CKE, CS, WE, CAS, and RAS signals. If a super self-refresh entry command (SSELF: see External Operation at a third line in Fig. 2) is obtained as a result of decoding, the input buffer circuit (COMMAND

DECODE) 8 delivers a start (START) instruction signal (ENCODE) to the ECC controller 6 as a control signal 1. The start instruction signal (ENCODE) is shown in a fourth line in Fig. 2 as a high-level part. At the time when the input buffer circuit (COMMAND [[BUFFER]] DECODE) 8 obtains the super self-refresh entry command (SSELF), supply of an external clock (CLK: see a second line in Fig. 2) to the SDRAM 10 is stopped. Supplied with the start instruction signal (ENCODE), the ECC controller 6 is supplied with an internal clock (ICLK: see a sixth line in Fig. 2). Supplied with the internal clock (ICLK), the ECC controller 6 delivers an operation mode signal 4 representative of encoding to the ECC-CODEC circuit 7.

**Please replace paragraph [0082] with the following rewritten paragraph:**

**[0082]** Supplied with the operation mode signal 4 representative of the encoding, the ECC-CODEC circuit 7 starts an encoding operation. Specifically, the ECC-CODEC circuit 7 generates parity data (check bits for error detection and correction) with reference to information data stored in [[ach]] each bank of [[th]] the memory and writes the parity data into a parity memory region (PARITY) of each bank of the memory (Parity Generation with Refresh: see Internal Operation at a tenth line (last line) in Fig. 2).

**Please replace paragraph [0091] with the following rewritten paragraph:**

**[0091]** Thus, the semiconductor integrated circuit device enters into an entry time (ENTRY-TIME depicted at the uppermost part in Fig. 2) when [[th]] the super self-refresh entry command (SSELF) is supplied from the outside. In the entry time, reading of all bits of the information data is executed and parity bits are generated and written. Subsequently, the semiconductor integrated circuit device proceeds to the super self-refresh (long-cycle self-refresh) depicted at the uppermost part in Fig. 2. The refresh is carried out in a long cycle beyond the capacity of the normal refresh and errors possibly generated are left.

**Please replace paragraph [0095] with the following rewritten paragraph:**

**[0095]** Referring to Figs. 4A and 4B, a FF (flip-flop) circuit used as each of the register circuits 13 through 17 comprises a switch 41 supplied with a signal at the Input-terminal IN and controlled by the clocks CLK and CLKB, a switch 42 supplied with an output signal of the switch 41 and controlled by the clocks CLK and CLKB, a switch 43 supplied with an output signal of the switch 42 and controlled by the clocks CLK and CLKB, and a switch 44 supplied with an output signal of the switch 43 and controlled by the clocks CLK and CLKB. An output signal of the switch 44 is delivered to the output terminal OUT. The FF circuit further comprises a NAND gate 45 supplied with the output signal of the switch 41 and a signal at the terminal CLRB, an inverter 46 for inverting an output signal of the NAND gate 45 and delivering an inverted signal to the switch 43 as an input signal, a NAND gate 47 supplied with the output signal of the switch 43 and the signal at the terminal CLRB, and an inverter 48 for inverting an output signal of the NAND gate 47 and delivering an ~~invert d~~ inverted signal to the output terminal OUT. An output signal of the NAND gate 47 is delivered to an output terminal OUTB.

**Please replace paragraph [0101] with the following rewritten paragraph:**

**[0101]** Referring to Fig. 3, the ECC controller 6 ~~compris s th~~ comprises the command generator 11, the address generator 12, and the output register circuit (~~flop-flop~~ flip-flop circuits) 13 to 17 as described above and serves to operate the SDRAM 10 (Fig. 1) and the ECC-CODEC circuit (coder/decoder circuit) 7 (Fig. 1) from the inside so as to carry out parity generation (Parity-Generation) and correcting operation (Correct) (see Fig. 2).

**Please replace paragraph [0105] with the following rewritten paragraph:**

**[0105]** The error detection signals (ERROR and LOCATION) 5 returned from the ECC-CODEC circuit 7 to the command generator 11 is transmitted through an output register circuit (78 in Fig. 22 which will later be described). A MA (main amplifier) output signal (output data) is first buffered in an output register (DATA OUTPUT REGISTER: see Fig. 1 and Figs. 17 and 18 which will later be described) and then delivered from a data output buffer circuit (DQ) to the outside. ~~Likewis~~ Likewise, the output data (MA output signal) supplied to the

ECC-CODEC circuit 7 is first buffered in an output register circuit (depicted by "FF" in Fig. 30 which will later be described). On the contrary, input data from a data input buffer circuit (DQ) are first buffered in an input register (DATA INPUT REGISTER: see Fig. 1 and Figs. 17 and 18 which will later be described) and then sent to a WB (write buffer). Likewise, the parity bits produced from the ECC-CODEC circuit 7 may be first buffered in the output register circuit and then sent to the WB to be written into memory cells. Strictly, whether the register is required or not depends upon an operation speed of the clock and the register is unnecessary in case of a low speed. No register is provided in Figs. 30 and 31 which will later be described.

**Please replace paragraph [0123] with the following rewritten paragraph:**

**[0123]** SSROP: To change [[th]] the internal operation ~~b tween~~ between four-bank simultaneous operation and one-by-one operation for [[on]] one bank at a [[tim ]] time. In the structure in Fig. 1 (also in the structure of Fig. 17 which will later be described), the ECC-CODEC circuit is arranged for each IO line. Therefore, no more than the one-by-one operation can be selected. On the other hand, in case of Fig. 18 which will later be described, the ECC-CODEC circuit is arranged for each MA/WB of each bank and the four-bank simultaneous operation can be selected. The four-bank simultaneous operation requires large current consumption but can shorten the coding/decoding time to 1/4.

**Please replace paragraph [0142] with the following rewritten paragraph:**

**[0142]** Referring to Fig. 6, the ECC-CODEC circuit 7 used in [[th]] the semiconductor integrated circuit device in Fig. 1 comprises a combination of a coder circuit and a decoder circuit.

**Please replace paragraph [0144] with the following rewritten paragraph:**

**[0144]** Figs. 7 and 8 [[shows]] show an example 1 of the super self-refresh internal operation carried out by the ECC-CODEC circuit 7 in Fig. 6. Fig. 7 shows the parity generation (1) (parity bit calculation) in the example 1 of the super self-refresh internal operation while Fig. 8 shows the parity generation (2) (parity bit writing) in the example 1 of the super self-refresh

internal operation. In synchronization with the internal clock (Internal CLK) within the device, commands of memory activation (ACTV) and reading operation (READ) are executed. Simultaneously, a row address (XA) and a column address (YA) are acquired. With reference to the addresses, Column (column address) is incremented and memory data of 1024 bits are read and taken into the main amplifier MA as read data. In addition, the read data are taken into the shift registers (S0-S15) of the circulating circuit 73 in Fig. 6 and subjected to calculation to produce the parity data based on the original memory data. In a following cycle, the parity data are delivered to the write buffer WB bit by bit. At this time, in synchronization with the internal clock (Internal CLK) within the device, commands of memory activation (ACTV) and writing ~~op ration~~ operation (WRIT) are executed. Simultaneously, the row address (XA) and the column address (YA) corresponding to the parity bit region are acquired. Based on these addresses, Column (column address) is incremented and 16 parity bits are written into the memory cells (corresponding to Hamming codes [1040, 1024] although not described in detail).

**Please replace paragraph [0147] with the following rewritten paragraph:**

**[0147]** Figs. 9 and 10 shows an example 2 of the super self-refresh internal operation carried out by the ECC-CODEC circuit 7 in Fig. 6. Fig. 9 shows the correcting operation (Correct) (1) (syndrome calculation) in the example 2 of the super self-refresh internal operation while Fig. 10 shows the correcting operation (Correct) (2) (error location detection and correction/writing) in the example 2 of the super self-refresh internal operation. In synchronization with the internal clock (Internal CLK) within the device, the original memory data and the parity data are read in [[th]] the manner described in conjunction with Figs. 7 and 8. The circulating circuit 73 in Fig. 6 carries out backward shift and logical operation to detect a defective address. With reference to the defective address, commands of memory activation (ACT) and reading operation (READ) are executed in synchronization with the internal clock (Internal CLK) within the device. The readout data appearing on the main amplifier MA are erroneous information. Therefore, the readout data are inverted and delivered to the write buffer WB. Simultaneously, a write command (WRIT) is produced and corrected data are written into a

corresponding address of the memory. Subsequently, the similar operation is repeated and correction of the error data is carried out for all bits.

**Please replace paragraph [0152] with the following rewritten paragraph:**

**[0152]** (4) After the SYNDROME signal is turned HIGH (CODEC syndrome mode), issuance of the internal operation commands <ACTIVE> <READ>. . . <PRE> is repeated as shown in Figs. 7 and 8. While X scanning is performed with [[th]] the burst length of 16 or 32, READ operation of 1024 bits is carried out. At this time, the CODECE signal is turned HIGH in synchronization with the output timing of the readout data. The shift registers are circularly shifted and the data of 1024 bits are successively taken into the CODEC bit by bit. Thus, the parity bits are calculated for the 1024 information bits and the result of calculation is retained in the shift registers of 16 bits as the parity bits of 16 bits. After completion, the CODEC mode signal is returned LOW.

**Please replace paragraph [0162] with the following rewritten paragraph:**

**[0162]** (6) After the CORRECT signal is turned HIGH (CODEC correction mode), the CODECE signal is turned HIGH without issuing the internal operation commands and (backward) cyclic shift of the shift registers alone is repeatedly carried out, as shown in Figs. 9 and 10. It is noted here that generation of [[th]] the internal addresses is executed in the manner reverse to that during the syndrome calculation in correspondence to the (backward) cyclic shift of the shift registers. At this time, the first (backward) cyclic shift corresponds to the syndrome pattern of the first bit (the last-acquired bit). In case where "the uppermost or most significant bit (S15) alone is 1 while the remaining bits are all zero", the bit is judged to be erroneous. Except for the case where "the uppermost or most significant bit (S15) alone is 1 while the remaining bits are all zero", the (backward) cyclic shift is repeated. If an erroneous bit is detected, the CODECE signal is turned LOW and the (backward) cyclic shift is stopped. The internal commands <ACTV> <READ> <WRIT> <PRE> are issued as illustrated in Figs. 9 and 10 and inversion (correction)/writing is executed.

**Please replace paragraph [0177] with the following rewritten paragraph:**

**[0177]** The control circuit produces the command signals (IRAS-IWE in Fig. 3) and the command address signals (IA(0)-IBA(1) in Fig. 3) of internal origin in the manner similar to deciding the operation mode within the device in accordance with external specification (i.e., logical levels of the command signals RAS, CAS, and WE and the command address signals (address signals not serving as conventional addresses indicating access addresses but serving as command signals for determining the operation modes in time division) supplied from the outside). These signals are latched in single-phase synchronization (synchronization with either one of rise and fall of the clock) with an external clock (or an internal clock derived therefrom) and serve to produce [[th]] the operation mode related to the super self-refresh. Preferably, the input buffer of the SDRAM selectively ~~acquir-s~~ acquires the command/address signals supplied from the outside or the command/address signals of internal origin and the operation in the device is determined as described above. The ECC controller 6 has a circuit structure at least including the command generator 11, the address generator (for generating the conventional address and the command address in time division) 12, and the output register circuits (latch or FF) 14 through 17.

**Please replace paragraph [0206] with the following rewritten paragraph:**

**[0206]** Referring to Fig. 15, the above-mentioned error recording circuit 24 is added to the ECC-CODEC circuit 7 in the semiconductor integrated circuit device in Fig. 1 so as to hold the H level output of the ERROR signal in DC. The ECC-CODEC circuit carries out error detection in the Correcting operation. This is applied to the BIST operation in the circuit illustrated in Fig. 15. In an error judging cycle (a cycle in which result of judgment of presence/absence of error is produced after completion of syndrome calculation of one code word), ECLK carries out clocking operation of one clock and the error recording circuit holds the ERROR signal as an ETRIG signal. When the ETRIG signal is changed from LOW to HIGH, the error state signal ESTATE is turned HIGH. This state is held unless a RESET signal is supplied. Thus, if the data read in the Correcting operation has an error even in one bit, the error [[stat]] state signal ESTATE is turned HIGH and held. Upon completion of the BIST operation,

the result ESTATE (see the ninth line in Fig. 13) is read from the error recording circuit 24 in response to the BIST exit command (BISTX: see the second line in Fig. 13) from the outside.

**Please replace paragraph [0209] with the following rewritten paragraph:**

**[0209]** With the above-mentioned structure, the error detection and correction functions for the memory data in the super self-refresh function are used and applied to the BIST circuit. When the BIST exit command (BISTX: see the second line in Fig. 13) is executed, the operation of detecting an error in the memory data is carried out by the above-mentioned self-test (self-test: see the last line in Fig. 13). Upon detection of the error, the ERROR signal is produced. In addition, although not shown in the figure, error location detection and correction can [[b]] be carried [[ut]] out and the self-test can be carried out.

**Please replace paragraph [0213] with the following rewritten paragraph:**

**[0213]** Referring to Fig. [[7]] 17, a semiconductor integrated circuit device according to another embodiment of this invention is shown. In the semiconductor integrated circuit device, the SDRAM [[10]] 10' is a 256-Mb SDRAM and has a word structure of x 16. The X address (including the bank address) is 15 bits in total. The Y address is 9 bits in total. The parity bit storage region is expanded in the X direction of each bank. In order to access to the parity bit storage region, 15 bits are insufficient for the X address and 16 bits (= 15 + 1) are used. Correspondingly, X address registers, X address lines, X (row) decoders, word drivers, and the like are increased in number.

**Please replace paragraph [0215] with the following rewritten paragraph:**

**[0215]** In the ECC-CODEC circuit 7, ECC-CODEC is disposed for each IO line. In this example, an internal I/O is 16 bits. Therefore, in [[th]] the ECC-CODEC circuit 7, 16 CODECs are disposed. The ECC-CODEC circuit 7 may be arranged in any location on the internal IO bus. The degree of freedom in layout is assured and chip-size overhead can be suppressed.

**Please replace paragraph [0216] with the following rewritten paragraph:**

**[0216]** Referring to Fig. 18, a semiconductor integrated circuit device according to still another embodiment of this invention is shown. In the semiconductor integrated circuit device, the SDRAM [[10]] 10" is a 256-Mb SDRAM and has a word structure of x 16 like in Fig. 17. However, the ECC-CODEC circuit 7 is arranged for each I/O of each memory bank. In this case, 16 ECC-CODECs are arranged in each ECC-CODEC circuit 7. Thus, the ECC-CODECs, 16 per bank and 64 in total, are arranged. This results in a disadvantage in view of chip-size overhead. The degree of freedom in layout is not achieved and the ECC-CODEC must be disposed near each MA (main amplifier) and each WB (write buffer).

**Please replace paragraph [0228] with the following rewritten paragraph:**

**[0228]** Supplemental description will be made in conjunction with Fig. 20. The expectation data are issued in synchronization with the <READ> command and adjusted in timing with the readout data by the use of DCLK. The result ERROR of comparison with the readout data is acquired by ECLK to become [[th]] the ETRIG signal. If the ETRIG signal is turned HIGH at least once, the error record signal ESTATE is ~~turn d~~ turned HIGH and is not erased unless it is reset. In this example, the fourth bit of the readout data is different from the expectation data and ESTATE of HIGH (occurrence of error) is recorded. Finally, the COMPARE signal is turned HIGH and ESTATE is read to the outside.

**Please replace paragraph [0233] with the following rewritten paragraph:**

**[0233]** Referring to Fig. 25, a CODEC-CLK generator circuit for supplying clocks (CCLK, CCLKB, CCLK2, CCLK2B) to the ECC-CODEC circuit 7 in Figs. 21 and 22 is shown. The CODEC-CLK generator circuit illustrated in Fig. 25 comprises a delay circuit DL1 including inverters in two stages and a delay circuit DL2 including inverters in four stages. A delay is produced between clock operation of CCLK and CCLKB and clock operation of CCLK2 and CCLK2B so as to assure an operation margin of the register circuits of a left/right shift type illustrated in Figs. 23A to 23C. [[Th]] The operation margin will be described in conjunction with Fig. 23A by way of example. The register circuit of a left/right shift type carries out shift

operation by the control clocks CCLK2 and CCLK2B for opening and closing two latch circuits on the left and the right and by the control clocks CCLK and CCLKB for copying the data of one latch circuit to the adjacent latch circuit. At first, when CCLK is changed from LOW to HIGH at first, the data in the left and the right latch circuits are the same. If CCLK2 is changed from LOW to HIGH later, no influence is given to the result. Next, when CCLK is returned from HIGH to LOW and if CCLK2 is returned from LOW to HIGH later, the right latch circuit is closed while the left latch circuit is opened. Therefore, the data are copied from the right latch circuit to the left latch circuit of the adjacent shift register so that the data flow from the right to the left. In other words, forward shift is not achieved. If CCLK2 is first returned from LOW to HIGH, the right latch circuit is opened and the left latch circuit is closed. Therefore, the data are copied from the left latch circuit in the adjacent shift register to the right latch circuit so that forward shift is carried out. In backward shift operation, CCLK and CCLKB are operated reversely in phase to CCLK2 and CCLK2B. In this case also, clock operation of CCLK2 and CCLK2B must be carried out first.

**Please replace paragraph [0240] with the following rewritten paragraph:**

**[0240]** On the other hand, the entry/exit scheme shown in Fig. 26 can be used by a user of the general-purpose SDRAM. Without having the commands for "super self-refresh", the normal self-refresh commands (self-refresh entry command (SELF: see External Operation at the third line in Fig. 26) and self-refresh exit command (SELFX: see External ~~Op ration~~ Operation at the third line in Fig. 26)) are directly used. Thus, the entry/exit scheme is basically similar to that for the self-refresh commands.

**Please replace paragraph [0250] with the following rewritten paragraph:**

**[0250]** Referring to Figs. 30 and 31, connection among the ECC controller 6 and the ECC-CODEC circuit 7 in the structure illustrated in Fig. 18 is shown in detail. The ECC controller 6 supplies the CODEC mode signal (INIT, PARITY, SYNDROME, CORRECT, CODECE) in common to the ECC-CODECs (Figs. 21 and 22), 64 in number. An ICLK generator supplies ICLK (internal synchronization clock signal) in common to the ECC

controller 6 (or 6' in Fig. 11) and the control logic 209 of the SDRAM. The ICLK generator is supplied with an oscillation start instruction (ICLKON of HIGH) from the control logic 209 of the SDRAM and starts oscillation. On the contrary, when an oscillation stop instruction (ICLKON of LOW) is supplied, the ICLK generator stops oscillation. As the clock signal to the ECC-CODECs, the ICLK is converted through a CCLK generator (Fig. 25) into four synchronization clocks (CCLK, CCLKB, CCLK2, CCLK2B) to be supplied to every four ECC-CODECs in common. Thus, for 16 ECC-CODECs per each bank, four CCLK generators (Fig. 25) are arranged. The clock signals to the ECC-CODECs are produced when the CODECE (codec enable) signal is HIGH. Per each bank, four clock signals are supplied and individually controlled by the ECC controller 6 if necessary so that the operation per bank is possible. The output of the MA (main amplifier) has two lines including a normal bus and an output bus to the ECC-CODEC which are switched in correspondence to the normal mode and the super self-refresh mode. The data read out in the normal mode are sent through the normal bus and a common I/O bus and buffered in the data output register to be delivered to the outside. The data read out in the parity generation/correcting operation in the super self-refresh mode pass through the output bus to the ECC-CODEC, buffered in the register circuit (FF in Fig. 30), and successively supplied to the shift registers in the ECC-CODEC. The WB (write buffer) also has two lines including a normal bus and an input bus from [[th]] the ECC-CODEC which are switched in correspondence to the normal mode and the super self-refresh mode. In the normal mode, write data supplied from the outside are buffered in the data input register and sent through the common I/O bus and the normal bus to be supplied to the WB (write buffer). In the parity generation in the super self-refresh mode, the parity bits produced from the ECC-CODEC pass through the input bus from the ECC-CODEC and supplied to the WB (write buffer). Although not shown in Figs. 30 and 31, the parity bits may be buffered in the register circuit and then supplied to the WB like in the normal mode. The ECC-CODEC supplies the error location detection signal LOCATION and the error detection signal ERROR to the ECC controller 6. The outputs of the ECC-CODECs, 16 in number, for each bank are subjected to OR operation to finally produce the error location detection signal LOCATION and the error detection signal ERROR for each bank. The error location detection signals LOCATION of four banks are

simply subjected to OR operation to produce a single LOCATION signal which is supplied to the ECC controller 6. On the other hand, the error detection signals ERROR are AND'ed with the bank enable signal BAE(j) activated in correspondence to the PASR (partial self refresh) mode to produce a single ERROR signal which is supplied to the ECC controller 6. For example, if the PASR mode indicates two banks, the bank enable signals BAE(0) and BAE(1) are HIGH and others are LOW. Only the error detection signals ERROR from the banks 0 and 1 are OR'ed and supplied to the ECC controller 6. In this manner, the ERROR signals of the banks 2 and 3 which are not guaranteed of operation can be neglected. Therefore, in the ECC controller 6, it is possible to omit issuance and operation of the useless internal commands in the Correcting operation.

**Please replace paragraph [0251] with the following rewritten paragraph:**

**[0251]** Next referring to Figs. 32 and 33, supplemental description will be made of the correcting operation in Figs. 9 and 10. Figs. 32 and 33 show the left half and the right half of details of operation (corresponding to [[th]] the correcting operation in Figs. 9 and 10) from the syndrome calculation to the error location detection in the super self-refresh operation in case where the ECC controller 6' in Fig. 11 and the ECC-CODEC circuit 7 in Figs. 21 and 22 are used.

**Please replace paragraph [0252] with the following rewritten paragraph:**

**[0252]** Output of the ECC controller 6' is carried out through the register circuits 14, 15, and 17. Therefore, the outputs of the command generator 11 and the address generator 12 are delayed by one cycle through the register circuits 14, 15, and 17. At first, in the syndrome calculation shown in Fig. 9, the stream of data is directed in one direction from the ECC controller to the control logic and the ECC-CODEC circuit. Therefore, only the output of the ECC controller is delayed by one cycle from the outputs of the command generator and the address generator, as in Fig. 9. The four clocks CCLK, CCLKB, CCLK2, CCLK2B supplied from the CCLK generator (Fig. 25) as a clock supplying circuit are set by the delay circuit DL1 (Fig. 25) so that the clocks CCLK and CCLKB are operated behind in comparison with the

clocks CCLK2 and CCLK2B to assure an operation margin of the cyclic shift operation of the ECC-CODEC circuit. If the delay relationship is reversed, the shift registers will destroy the data. After completion of the issuance of the command of the syndrome calculation, the command generator accepts the error detection signal ERROR (ERROR Detect). In this event, the command generator waits the error detection signal ERROR with a margin for the delay time required for the error detection signal ERROR to reach the ECC controller after the outputs of the 64 ECC-CODEC circuits are produced and OR'ed. In the example illustrated in Figs. 32 and 33, the error detection signal ERROR is received at a third cycle from the issuance of the last <PRE> command. If the error detection signal ERROR is HIGH, the ECC controller proceeds to the error location detection in the following manner. At first, the CORRECT signal is turned HIGH and CCLK and CCLKB are ~~inv rted~~ inverted and outputted irrespective of ICLK. In this operation, the data memorized in the shift register circuit (Fig. 23) are processed in the following manner. The data memorized in the left latch circuit are copied to the right latch circuit so that the data in the left and the right latch circuits become identical. In a next one cycle, the SYNDROME signal is turned LOW and the four clocks CCLK, CCLKB, CCLK2, CCLK2B are inverted. Simultaneously, CORRECTB is inverted and backward cyclic shift of one bit is carried out. Again, the clocks CCLK and CCLKB are operated behind in comparison with the clocks CCLK2 and CCLK2B to assure an operation margin of the shift operation. This is assured by the delay circuit DL2 of the CCLK generator (Fig. 25) as a clock supplying circuit. The delay relationship is always maintained also in subsequent clocking operations by the delay circuit DL1 of the CCLK generator (Fig. 25) as a clock supplying circuit. By controlling the SYNDROME and the CORRECT signals, the ECC-CODEC circuit proceeds from the syndrome mode into the correction mode. CCLK and CCLKB are reverse in phase to CCLK2 and CCLK2B so that backward cyclic shift can be carried out. By the one-bit shift mentioned above, the syndrome pattern for the bit read out from the memory cells at the last of the syndrome calculation appears in the shift registers of 16 bits in the ECC-CODEC. When only the uppermost or most significant bit is HIGH and the remaining bits are LOW, the error location detection signal LOCATION is HIGH and the ECC controller detects that the bit in question is in error. In order to carry out error judgment for a subsequent readout bit, the CODECE (codec enable) signal is

turned HIGH. The four clocks CCLK, CCLKB, CCLK2, CCLK2B are supplied from the CCLK generator (Fig. 25) as the clock supplying circuit. Backward cyclic shift is carried out and error detection in the subsequent readout bit is performed. In parallel, the address generator carries out backward shift of the internal address. The backward shift of the address is started three cycles after the CODECE (codec enable) signal is turned HIGH. In case where the error location detection signal LOCATION is turned HIGH as a result of the subsequent backward cyclic shift of [[th]] the shift registers, the ECC controller is ~~responsiv~~ responsive to the error location detection signal LOCATION and turns the CODECE signal into LOW to stop the operation of the ECC-CODEC circuit. At first, in a cycle of receiving the LOCATION signal, one-cycle cyclic shift is carried out. Furthermore, since the output of the command generator is produced through the register circuits, the stop of the ECC-CODEC circuit is delayed by one cycle. The error location detection signal LOCATION is produced also through the registers and is therefore produced from the ECC-CODEC circuit with one-cycle delay. Therefore, the result of judgment one bit before is seen. Thus, the error location detection is delayed by three cycles. Therefore, the ECC-CODEC circuit (Figs. 21 and 22) has three registers memorizing the LOCATION signal to memorize previous values back to the value (L3) three [[cycle]] cycles before. By the value, inversion of the rewritten data is controlled (76 in Fig. 22). For this purpose, the address generator delays the internal address backward shift operation by three cycles. Supplied with the error location detection signal LOCATION of HIGH, the ECC controller issues the internal commands for stopping backward shift operation of the ECC-CODEC circuit and the address generator and for inverting the error bit and rewriting the corrected bit. By the delay control mentioned above, error judgment of the bit in question and the address are coincident and the error correction can properly be carried out. The ECC controller finishes the issuance of the internal command and, for a next error location detection, the backward cyclic shift of the ECC-CODEC circuit and backward shift operation of the address generator are started. Herein, the delay relationship by the three cycles is maintained.